Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An apparatus comprising:

core control logic to provide a data signal; and

output drive logic including a local data latch and a transmitter, the data latch to receive the data signal and to provide true and complementary forms of the data signal to the transmitter over symmetrical signal paths, the transmitter to provide an output signal to an external receiver.

2. (Canceled)

3. (Original) The apparatus of claim 1 further comprising

design for testability (DFT) logic local to the transmitter, the DFT logic including an internal receiver coupled to an output of the transmitter and a local DFT latch coupled to an output of the internal receiver.

4. (Original) The apparatus of claim 3 wherein the internal receiver comprises a dual oxide sense amplifier.

5. (Original) The apparatus of claim 4 wherein the dual oxide sense amplifier includes precharge logic to precharge input lines to the dual oxide sense amplifier to a first voltage level.

6. (Original) The apparatus of claim 5 wherein the dual oxide sense amplifier is clocked.

7. (Original) The apparatus of claim 5 wherein the dual oxide sense amplifier is capable of operating in response to low voltage swing, differential input signals.

8.-29. (Canceled)

30. (New) The apparatus of claim 1 wherein the core control logic is video control logic.

31. (New) The apparatus of claim 3 wherein the internal receiver is to compare an output of the transmitter with a reference voltage and the local DFT latch is to latch a result of the comparison.

32. (New) An apparatus comprising:

core control logic to provide a data signal;

a data transmission output driver including a local data latch and a transmitter, the data latch to latch data from the core control logic destined for the transmitter, the transmitter to be coupled to an external receiver; and

design for testability (DFT) logic including an internal receiver and a local DFT latch, the internal receiver to compare an output of the transmitter with a reference voltage, the local DFT latch to latch a result of the comparison.

33. (New) The apparatus of claim 32 further comprising true and complementary signal paths between the data latch and the transmitter, the true and complementary signal paths being substantially symmetrical.

34. (New) The apparatus of claim 32 wherein the core control logic is video core control logic.

35. (New) The apparatus of claim 32 wherein the internal receiver comprises two dual oxide sense amplifiers, a first dual oxide sense amplifier to receive a true form of the transmitter output, a second dual oxide sense amplifier to receive a complementary form of the transmitter output.

36. (New) The apparatus of claim 35 wherein the signal lines of the dual oxide sense amplifiers are to be precharged prior to sensing.

37. (New) The apparatus of claim 35 wherein the dual oxide sense amplifiers are to receive two different, non-ground supply voltages.

38. (New) The apparatus of claim 35 wherein at least one of the dual oxide sense amplifiers includes

a sensing circuit having differential input bit lines, the sensing circuit to sense a low voltage swing signal in response to an enable signal;

a precharge circuit to precharge the input bit lines; and

a high voltage conversion circuit to receive an input signal having a first voltage swing and to provide the enable signal having a larger voltage swing,

the at least one dual oxide sense amplifier including at least a first transistor having a gate oxide of a first thickness and a second transistor having a gate oxide of a second thickness greater than the first thickness.

39. (New) A method comprising:

receiving video data from core control logic at a latch;

transmitting true and complementary forms of the video data from the latch to a local transmitter over symmetrical signal paths; and

providing output data from the transmitter to an external receiver.

40. (New) The method of claim 39 further comprising:

receiving the output data from the transmitter at an internal receiver;

comparing the output data to a reference signal;

locally latching an output of the internal receiver;

amplifying the output of the internal receiver; and

providing the amplified output of the internal receiver to the core control logic.